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2823

**TRANSMITTAL LETTER  
(General - Patent Pending)**

Docket No.  
END920010026US1

In Re Application Of: **Bernier et al.**

Serial No.  
**09/885,853**

Filing Date  
**6/20/2001**

Examiner  
**William D. Coleman**

Group Art Unit  
**2823**

Title: **EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL TO CHIP CONNECTION**



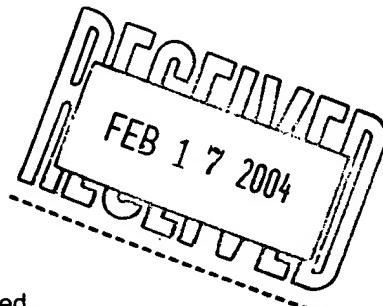
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**Request for Re-Instatement of Appeal- 1 page  
Supplemental Brief-22 pages**

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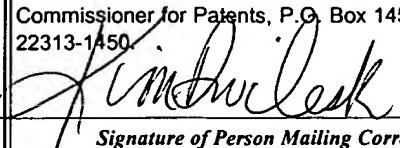
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Dated: **2/2/2004**

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# THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Bernier *et al.*

Art Unit: 2823

Serial No.: 09/885,853

Dkt. No.: END920010026US1

Filed: 6/20/01

Examiner: William D. Coleman

Title: **EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL TO CHIP CONNECTION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

## Request for Re-Instatement of Appeal Under 37 CFR §1.93(b)(2)

Applicants request Re-Instatement of the Appeal from the rejection of the Examiner dated April 10, 2003, in light of the Office Action mailed November 25, 2003. Submitted herewith is a Supplemental Appeal Brief which addresses the rejection of claims in the Office Action mailed November 25, 2003.

Respectfully submitted,

  
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Dated: 02/02/2004

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09/885,853



**THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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**SUPPLEMENTAL BRIEF OF APPELLANTS**

This Supplemental Appeal Brief, pursuant to the Office Action mailed November 25, 2003, pertains to the appeal from the rejection of the Examiner dated April 10, 2003. The previously submitted Appeal Brief filed September 8, 2003 is incorporated, in its entirety, herein by reference. The present Supplemental Appeal Brief addresses the rejections of claims in the Office Action mailed November 25, 2003.

**REAL PARTY IN INTEREST**

International Business Machines, Inc. is the real party in interest.

**RELATED APPEALS AND INTERFERENCES**

None.

09/885,853

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## **STATUS OF CLAIMS**

Claims 1-18 and 20-40 are currently pending. Claims 21-40 are withdrawn. Claims 7 and 8 are allowed.

## **STATUS OF AMENDMENTS**

There are no After-Final Amendments which have not been entered.

## **SUMMARY OF INVENTION**

The present invention discloses an electronic structure, comprising a semiconductor substrate having a first electrically conductive pad thereon, an organic substrate having a second electrically conductive pad thereon, and a solder member electrically coupling the first pad to the second pad. See FIG. 1 and specification, page 3, lines 10-15. A surface area of the first pad exceeds a surface area of the second pad. See specification, page 5, line 21 - page 6, line 2.

The surface area of the first pad may exceed the surface area of the second pad by a factor of at least about 1.2. The surface area of the first pad may exceed the surface area of the second pad by a factor between about 1.1 and about 1.3. the first pad may exceed the surface area of the second pad by a factor of at least about 1.2. The surface area of the first pad may exceed the surface area of the second pad by a factor between about 1.3 and about 2.0.

See specification, page 8, lines 5-9.

The coefficient of thermal expansion (CTE) of the organic substrate mat be between

about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C. See specification, page 4, lines 3-4.

P may be between about .15 and about .75, wherein P is defined as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder member, wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the semiconductor substrate. See specification, page 11, lines 3-12.

The organic substrate may include an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof. See specification, page 3, line 19 - page 4, line 2.

The solder member may include a controlled collapse chip connection (C4) solder ball, and the solder member may include a lead-tin alloy. See specification, page 4, lines 5-8.

A distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate may be at least about 0.25 mm. See specification, page 6, lines 2-4. The distance from the centerline of the solder member to the closest lateral edge of the semiconductor substrate may be at least about 0.40 mm. See specification, page 10, lines 14-15.

The electronic structure may further comprise an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal. See FIG. 1 and specification, page 4, lines 13-15.

## **ISSUES**

1. Whether claims 1, 2, 4, 9-13, 15 and 20 are unpatentable under 35 U.S.C. §103(a) over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Tung (U.S. Patent 6,592,019B2).
2. Whether claims 3, 5,-6, 14, and 16-17 are unpatentable under 35 U.S.C. §103(a) over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Tung et al. (U.S. Patent 6,592,019B2) as applied to claims 1, 2 and 4, and further in view of Chung (U.S. Patent 6,399,178B1).
3. Whether claim 18 is not unpatentable under 35 U.S.C. §103(a) over Zhang et al. (U.S. Patent 6,310,403 B1) in view of Chung, (U.S. Patent 6,399,178 B1).

## **GROUPING OF CLAIMS**

The claims are grouped as shown in Table 1:

Table 1

Group	Claims	Do Claims of Group Stand or Fall Together?
1	1-6 and 13-17	Yes
2	9-11	Yes
3	12	Yes
4	18	Yes
5	20	Yes

The claims of Group 2 do not stand and fall together with the claims of Group 1, because

the claims of Group 2 include the following issue not present in any of the claims of Group 1: whether the condition of a surface area of the first pad exceeding a surface area of the second pad by a factor (of at least about 1.2, between about 1.1 and about 1.3, or between about 1.3 and about 2.0) is obvious over Zhang in view of Tung.

The claims of Group 3 does not stand and fall together with the claims of Groups 1-2, because the claim of Group 3 includes the following issue not present in any of the claims of Groups 1-2: whether the condition of a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate being at least about 0.25 mm is obvious over Zhang in view of Tung.

The claim of Group 4 does not stand and fall together with the claims of Groups 1-3, because the claim of Group 4 is being rejected over different references (i.e., over Zang in view of Chung) than are the claims of Groups 1-3.

The claim of Group 5 does not stand and fall together with the claims of Groups 1-4, because the Examiner rejected the claim of Group 5 without providing any argument for the rejection and without providing any references to support the rejection, which did not occur for Groups 1-4.

## **ARGUMENT**

### **Issue 1**

#### **CLAIMS 1, 2, 4, 9-13, 15, AND 20 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER ZHANG ET AL. (U.S. PATENT 6,310,403B1) IN VIEW OF TUNG (U.S. PATENT 6,592,019B2).**

The Examiner rejected claims 1, 2, 4, 9-13, 15 and 20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Zhang et al. (U.S. Patent 6,310,403B1) in view of Tung (U.S.

Patent 6,592,019B2).

Claim 1

Appellants respectfully contend that claim 1 is not unpatentable over Zhang et al. in view of Tung, because Zhang in view of Tung does not teach or suggest each and every feature of claim 1. For example, Zhang in view of Tung does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad.”

The Examiner admits that “Zhang fails to teach wherein a surface area of the first pad exceeds a surface area of the second pad.” The Examiner alleges that “Tung teaches wherein a surface area of the first pad exceeds a surface area of the second pad. See FIG. 1B of Tung.”

In response to the preceding argument by the Examiner, Appellants note that the Examiner has not identified a first pad and a second pad in FIG. 1B of Tung, and has not provided any analysis of FIG. 1B of Tung. Appellants assume, however, that the Examiner is impliedly asserting that the copper contact 24 in FIG. 1B of Tung represents the first pad of claim 1 and that the copper contact 22 in FIG. 1B of Tung represents the second pad of claim 1. Appellants also note that FIG. 1B of Tung is a cross-sectional view which does not show the spatial extent of surfaces extending normal to said cross-sectional view. Therefore, since only a linear dimension and not a surface area is shown for contacts 24 and 22 in FIG. 1B of Tang, it is impossible to deduce relative surface areas contacts 22 and 24 from FIG. 1B of Tung. Therefore, Appellants contend that Tang does not teach or suggest that a surface area of the first pad exceeds a surface area of the second pad as required by claim 1.

Additionally, Appellants respectfully contend that it is not obvious to combine Tung with

Zhang in relation to claim 1, even if Tung were to teach or suggest the preceding feature of claim 1 (which Tung doesn't).

As a first reason why it is not obvious to combine Tung with Zhang in relation to claim 1, Appellants respectfully contend that having the surface area of the first pad exceed the surface area of the second pad is incompatible with Zhang who discloses in the very opposite. In FIG. 3, Zhang depicts the surface area of the first pad (between portion 171 and bump 181) is being smaller than the surface area of the second pad 191. Therefore, having the surface area of the first pad exceed the surface area of the second pad would destroy the teaching in FIG. 3 of Zhang.

As a second reason why it is not obvious to combine Tung with Zhang in relation to claim 1, Appellants respectfully contend that having the surface area of the first pad exceed the surface area of the second pad 191 would offer no utility to Zhang. Zhang's invention is directed to connecting the substrates 120 and 190 such that the respective interconnects in the substrates 120 and 190 are correctly aligned with each other, and Zhang teaches how to accomplish said alignment in col. 5, lines 27-36. Appellants maintain that having the surface area of the first pad exceed the surface area of the second pad 191 would not improve said alignment process or provide any other benefit to Zhang, since Zhang teaches a highly successful method of connecting the substrates 120 and 190 with each other.

As a third reason why it is not obvious to combine Tung with Zhang in relation to claim 1, Appellants respectfully contend that the Examiner has not presented a persuasive reason for modifying Zhang with Tung. The Examiner argues: "In view of Tung, it would have been obvious to one of ordinary skill in the art to incorporate the surface area of the first pad

exceeding a surface area of the second pad in the Zhang semiconductor device because the invention should not fail with the given geometry illustrated (column 7, line 9)."

In response to the preceding argument by the Examiner, Appellants respectfully contend that the Examiner has not provided any analysis to show the relevance of the preceding reason to Zhang. Additionally, the Examiner has not provided any analysis to show the relevance of the preceding reason to the requirement in claim 1 of having the surface area of the first pad exceed the surface area of the second pad, wherein said requirement in claim 1 is what prompted the Examiner to modify Zhang with Tung.

Moreover, the citation in col. 7, line 9 relied upon by the Examiner has no relevance to the relative surface areas of the contacts 24 and 22 of FIG. 1B of Tung. Indeed, Tung explains that Tung's invention will not fail specifically because of the length of the elongated pillars which has nothing to do with the relative surface areas of the contacts 24 and 22. Specifically, Tung states:

"As shown in FIGS. 5A and 5B, the peak shear stress at the edge of the die is less than the shear strength of copper so that **the elongated pillars of this invention should not fail with the given geometry illustrated, or similar geometries, due to shear stress**. FIGS. 6A and 6B illustrate similar data to those shown in FIGS. 5A and 5B but where the pillar height or length is 120 microns instead of 100 microns. A comparison of FIGS. 6A and 6B to those of FIGS. 5A and 5B will illustrate that **the longer the pillars, the less will be the shear stress experienced at the edge of the die and the interconnects connected to the die**"

(emphasis added). See Tung, col. 7, lines 6-16.

Based on the preceding arguments, Appellants maintain that claim 1 is not unpatentable over Zhang in view of Tung under 35 U.S.C. §103(a).

Claims 2, 4, 13, and 15

Since claims 2, 4, 13, and 15 depend from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claims 2, 4, 13, and 15 are not unpatentable under 35 U.S.C. §103(a).

Claim 9

Since claim 9 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 9 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 9 is not unpatentable over Zhang et al. in view of Tung, because Zhang in view of Tung does not teach or suggest each and every feature of claim 9. For example, Zhang in view of Tung does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2”.

The Examiner admits that “the combined teachings [of Zhang and Tung] fail to disclose the dimensions of the first and second pad surface area”. The Examiner argues: “However, the combined teachings fail to disclose the dimensions of the first and second pad surface area. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) “It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom.”

In response to the preceding argument by the Examiner, Appellants point out that the ratio  $S_1/S_2$ , where  $S_1$  and  $S_2$  is the surface area of first pad and second pad, respectively, is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 6, lines 7-13 for a discussion of how  $S_1/S_2$  affects said fatigue life. See Specification, page 6, line 14 - page 8, line 9 for a discussion of test data demonstrating the effect on fatigue life of varying  $S_1/S_2$ . Accordingly, Appellants maintain that claimed ranges of  $S_1/S_2$  is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 9 is not unpatentable over Zhang in view of Tung. Accordingly, Appellants contend that rejection of claim 9 should therefore be reversed.

#### Claim 10

Since claim 10 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 10 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 10 is not unpatentable over Zhang et al. in view of Tung, because Zhang in view of Tung does not teach or suggest each and every feature of claim 10. For example, Zhang in view of Tung does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3”.

The Examiner admits that “the combined teachings [of Zhang and Tung] fail to disclose the

dimensions of the first and second pad surface area". The Examiner argues: "However, the combined teachings fail to disclose the dimensions of the first and second pad surface area. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom."

In response to the preceding argument by the Examiner, Appellants point out that the ratio  $S_1/S_2$ , where  $S_1$  and  $S_2$  is the surface area of first pad and second pad, respectively, is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 6, lines 7-13 for a discussion of how  $S_1/S_2$  affects said fatigue life. See Specification, page 6, line 14 - page 8, line 9 for a discussion of test data demonstrating the effect on fatigue life of varying  $S_1/S_2$ . Accordingly, Appellants maintain that claimed ranges of  $S_1/S_2$  is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 10 is not unpatentable over Zhang in view of Tung. Accordingly, Appellants contend that rejection of claim 10 should therefore be reversed.

#### Claim 11

Since claim 11 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 11 is not unpatentable under

35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 11 is not unpatentable over Zhang et al. in view of Tung, because Zhang in view of Tung does not teach or suggest each and every feature of claim 10. For example, Zhang in view of Tung does not teach or suggest “wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0”.

The Examiner admits that “the combined teachings [of Zhang and Tung] fail to disclose the dimensions of the first and second pad surface area”. The Examiner argues: “However, the combined teachings fail to disclose the dimensions of the first and second pad surface area. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom."

In response to the preceding argument by the Examiner, Appellants point out that the ratio  $S_1/S_2$ , where  $S_1$  and  $S_2$  is the surface area of first pad and second pad, respectively, is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 6, lines 7-13 for a discussion of how  $S_1/S_2$  affects said fatigue life. See Specification, page 6, line 14 - page 8, line 9 for a discussion of test data demonstrating the effect on fatigue life of varying  $S_1/S_2$ . Accordingly, Appellants maintain that claimed ranges of  $S_1/S_2$  is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 11 is not unpatentable over Zhang in view of Tung. Accordingly, Appellants contend that rejection of claim 11 should therefore be reversed.

#### Claim 12

Since claim 12 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 12 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that claim 12 is not unpatentable over Zhang et al. in view of Tung, because Zhang in view of Tung does not teach or suggest each and every feature of claim 10. For example, Zhang in view of Tung does not teach or suggest “wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm”.

Appellants point out that the Examiner has not provided any argument that Zhang in view of Tung teaches or suggests the preceding feature of claim 12. In fact, the Examiner has not even alleged that Zhang in view of Tung teaches or suggests the preceding feature of claim 12.

Appellants point out that the distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is a novel feature of the present invention relating to extending fatigue life of the interface between the solder member and the first pad. See Specification, page 8, line 10 - page 10, line 19 for a discussion of test data demonstrating the effect on fatigue life of varying the distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate. Accordingly, Appellants maintain that claimed

ranges relating to said distance is novel and not obvious and not ascertainable by routine experimentation.

Based on the preceding arguments, Appellants respectfully maintain that claim 12 is not unpatentable over Zhang in view of Tung. Accordingly, Appellants contend that the rejection of claim 12 should therefore be reversed.

### Claim 20

Since claim 20 depends from claim 1, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claim 20 is not unpatentable under 35 U.S.C. §103(a).

In addition, Appellants respectfully contend that the Examiner has not presented any argument in support of the rejection of claim 20. Thus, Appellants contend that the Examiner has not made a *prima facie* case for obviousness in relation to claim 20 and the rejection of claim 20 should therefore be reversed.

### Issue 2

#### **CLAIMS 3, 5- 6, 14, and 16-17 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER ZHANG ET AL. (U.S. PATENT 6,310,403B1) IN VIEW OF TUNG ET AL. (U.S. PATENT 6,592,019B2), AND FURTHER IN VIEW OF CHUNG (U.S. PATENT 6,399,178 B1).**

The Examiner rejected claims 3, 5, 6, 14, and 16-17 under 35 U.S.C. §103(a) in view of Tung et al. (U.S. Patent 6,592,019B2), and further in view of Chung (U.S. Patent 6,399,178B1).

Since claims 3, 5, and 6 depend from claim 1, which Appellants have argued *supra* to be

patentable under 35 U.S.C. §103(a), Appellants maintain that claims 3, 5, and 6 are not unpatentable under 35 U.S.C. §103(a).

Since claims 14, 16, and 17 depend from claim 12, which Appellants have argued *supra* to be patentable under 35 U.S.C. §103(a), Appellants maintain that claims 14, 16, and 17 are not unpatentable under 35 U.S.C. §103(a).

### **Issue 3**

#### **CLAIM 18 IS NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER ZHANG ET AL. (U.S. PATENT 6,310,403B1) IN VIEW OF CHUNG (U.S. PATENT 6,399,178B1).**

The Examiner rejected claim 18 under 35 U.S.C. §103(a) as allegedly being unpatentable over Zhang et al. (U.S. Patent 6,310,403B1) in view of Chung (U.S. Patent 6,399,178B1).

Appellants respectfully contend that claim 18 is not unpatentable over Zhang in view of Chung, because Zhang in view of Chung does not teach or suggest each and every feature of claim 18. For example, Zhang in view of Chung does not teach or suggest “wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm”. The Examiner has presented no argument supporting that Zhang in view of Chung teaches or suggests the preceding feature of claim 18. In fact, the Examiner admits that “Zhang fails to disclose the dimensions ....” Thus, Appellants contend that the Examiner has not made a *prima facie* case for obviousness in relation to claim 18 and the rejection of claim 18 is therefore improper.

Additionally, Zhang in view of Chung does not teach or suggest “wherein the underfill material has an elastic modulus of at least about 1 gigapascal”. The Examiner admits that “Zhang

fails to disclose ... wherein the underfill material has an elastic modulus of at least about 1 gigapascal." The Examiner alleges that "Chung discloses an underfill material with an elastic modulus of at least about 1\_ gigapascal. Although Chung discloses the elastic modulus of the underfill material in units of psi (i.e., 2,000,000 psi, column 18, line 61) it is equivalent to Appellants units. In view of Chung, it would have been obvious to one of ordinary skill in the art to incorporate the elastic modulus of Chung into the Zhang semiconductor device because the rigid adhesive underfill perform is aligned with the substrate (column 14, lines 48-53)."

Appellants note that column 14, lines 48-53 of Chung states: "Rigid adhesive underfill preform 110 is aligned with substrate 30 so that the pattern of solder columns 134 of preform 110 corresponds with the pattern of contact pads 132 of substrate 30." Thus, column 14, lines 48-53 of Chung merely describes how rigid adhesive underfill preform 110 is aligned with substrate 30, but does not provide a reason for the modulus of at least about 1 gigapascal as required by claim 18. Moreover, the preceding statement in Chung does not provide any motivation for a modulus of at least about 1 gigapascal in the underfill 310 in Zhang, and the Examiner has provided no analysis to support why a person of ordinary skill in the art would use an underfill having modulus of at least about 1 gigapascal in the underfill 310 in Zhang. In col. 6, lines 6-10, Zhang states: "after the assembly process, an underfill material 310 is dispensed or injected between substrates 110 and 190 to package or encapsulate the interconnect bumps and the first and second pluralities of interconnects. Material 310 protects the bumps from becoming over stressed during subsequent temperature cycles." Appellants contend that there is no reason, based on the preceding statement in Zhang, why a person of ordinary skill in the art would use an underfill having modulus of at least about 1 gigapascal in the underfill 310 in Zhang. Thus, the

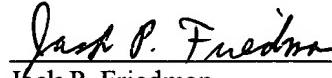
combination of Zhang and Chung is not obvious.

Based on the preceding arguments, Appellants respectfully maintain that claim 18 is not unpatentable over Zhang in view of Chung, and that the rejection of claim 18 should be reversed.

## SUMMARY

In summary, Appellants respectfully request reversal of the rejection of claims 1-6 and 9-18, and 20 under 35 U.S.C. §103(a).

Respectfully submitted,

  
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**THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Bernier *et al.*

Art Unit: 2823

Serial No.: 09/885,853

Dkt. No.: END920010026US1

Filed: 6/20/01

Examiner: William D. Coleman

**Title: EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL TO CHIP CONNECTION**

Commissioner for Patents

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**APPENDIX - CLAIMS ON APPEAL**

1. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

a solder member electrically coupling the first pad to the second pad.

2. The electronic structure of claim 1, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.

3. The electronic structure of claim 1, wherein P is between about .15 and about .75, wherein P is defined as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder member, wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the semiconductor substrate.

4. The electronic structure of claim 1, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

5. The electronic structure of claim 1, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

6. The electronic structure of claim 1, wherein the solder member includes a lead-tin alloy.

9. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2; and

a solder member electrically coupling the first pad to the second pad.

10. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.1 and about 1.3; and

a solder member electrically coupling the first pad to the second pad.

11. An electronic structure, comprising:
- a semiconductor substrate having a first electrically conductive pad thereon;
  - an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad by a factor between about 1.3 and about 2.0; and
  - a solder member electrically coupling the first pad to the second pad.
12. An electronic structure, comprising:
- a semiconductor substrate having a first electrically conductive pad thereon;
  - an organic substrate having a second electrically conductive pad thereon; and
  - a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.
13. The electronic structure of claim 12, wherein a coefficient of thermal expansion (CTE) of the organic substrate is between about 10 ppm/ $^{\circ}$ C and about 18 ppm/ $^{\circ}$ C.
14. The electronic structure of claim 12, wherein P is between about .15 and about .75, wherein P is defined as  $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$ , wherein  $C_{SOLDER}$  is a CTE of the solder member, wherein  $C_{ORGANIC}$  is a CTE of the organic substrate, and wherein  $C_{SEMI}$  is a CTE of the semiconductor substrate.

15. The electronic structure of claim 12, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

16. The electronic structure of claim 12, wherein the solder member includes a controlled collapse chip connection (C4) solder ball.

17. The electronic structure of claim 12, wherein the solder member includes a lead-tin alloy.

18. An electronic structure, comprising:

a semiconductor chip having a first electrically conductive pad thereon;

an organic chip carrier having a second electrically conductive pad thereon;

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm; and

an underfill material between the semiconductor chip and the organic chip carrier, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

20. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.40 mm.